REMARKS

This application has been reviewed in light of the Office Action dated October 31, 2005. Claims 1-4 and 6-12 are pending in this application. Claims 1-4 and 8-11, the independent claims, have been amended to define still more clearly what Applicant regards as his invention. Favorable reconsideration is requested.

Claims 1-4 and 6-12 were rejected under 35 U.S.C. § 103(a) as being obvious from European Patent Application 0905978 A2 to Yip et al. ("Yip EU") in view of Australian Patent Publication 199957151 A1 to Yip et al. ("Yip AU").

Claim 1 is directed to a data transfer circuit for transferring a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory for coding by a bit-plane coding processor. Detection means detects a maximum value in the data group as a transfer object, in which the detecting processing by the detection means is performed while transferring the data group and completed before completion of the transfer. Specifying means specifies a non-zero highest-order bit position among bits constructing the maximum value detected by the detection means, and outputs a code representing the bit position specified by the specifying means to the bit-plane coding processor. A bit in a position higher than the highest-order bit position specified by the specifying means is omitted from coding executed by the bit-plane coding processor after transferring the data group to the second memory.

Among the notable features of Claim 1 are that a data transfer

circuit transfers a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory, detects a maximum value in the data group as a transfer object, and specifies a non-zero highest-order bit position among bits constructing the detected maximum value.

Yip EU relates to data compression, and in particular to an architecture for encoding coefficients that have been constructed as a result of a compression process. Fig. 3 of that patent relates to a method of representing, or encoding, an image. At page 5, the Office Action states that "Yip EU does not appear to disclose transferring 'from a first memory to a second memory for coding'". The Office Action also states, at page 5, that "Yip EU also does not disclose detecting 'while transferring the data group and completed before completion of the transfer'".

Yip AU relates to an encoding method and apparatus for representing a digital image. In order to perform bit-plane coding, data transformation processing (606) and data analyzing (608-0...15) are executed for all bit-planes, upon transferring from a memory (612 as shown in Fig. 6) to another memory (614,616, 618-0...15).

More specifically, after multi-valued data stored in a memory (612 as shown in Fig. 6) is converted to bit-plane data by a bit-plane converter (606), the converted bit-plane data is written in another memory (614 or 616). Also, after multi-valued data stored in a memory (612 as shown in Fig. 6) is converted to bit-plane tree data by a bit-plane tree builder (608-0...15), the converted bit-plane tree data is written in another memory (618-0...15).

Thus, Yip AU needs all of bit-planes for encoding.

On the other hand, in Claim 1, while transferring a data group having data represented by plural bits stored in a first memory to a second memory, without changing the arrangement of a sequence of the plural bits, a maximum value in the data group is detected and then a non-zero highest-order bit position among bits constructing the maximum value is specified. Thus, upon bit-plane coding, since a bit-plane coding processor codes only each bit in each position lower than the highest-order bit position, the number of bit-plane to be coded can be reduced.

Nothing in Yip EU or Yip AU, whether considered either separately or in any permissible combination (if any) would teach or suggest a data transfer circuit that transfers a data group having data represented by plural bits, without changing an arrangement of a sequence of the plural bits, from a first memory to a second memory, detects a maximum value in the data group as a transfer object, and specifies a non-zero highest-order bit position among bits constructing the detected maximum value, wherein a bit in a position higher than the highest-order bit position specified is omitted from coding executed by the bit-plane coding processor after transferring the data group to the second memory, as recited in Claim 1.

Accordingly, Claim 1 is believed to be patentable over Yip EU and Yip AU, whether considered either separately or in any permissible combination (if any).

Independent Claims 2-4 and 8-11 recite certain features which are similar in many relevant respects to those discussed above with respect to Claim 1 and therefore are also believed to be patentable over Yip EU and Yip AU for at least the reasons discussed above.

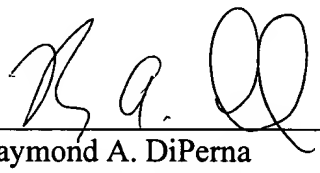
A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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